UM10178

25 A LFPAK demonstration board

Rev. 01 — 2 March 2006 User manual

Document information

Info	Content
Keywords	LFPAK, FET, demo board
Abstract	The 25 A LFPAK demo board is a single-phase buck converter design to demonstrate the performance of Philips LFPAK MOSFETs in a small form factor Point-of-Load (PoL) circuit. The very small 2.5 cm × 5.0 cm (1 in. × 2 in.), four layer board converts 12 V nominal input to 1.2 V nominal output and is capable of output currents of 25 A while maintaining case temperatures at or below 90 °C with a minimal 1.0 m/s (200 LFM) airflow at 25 °C ambient. Efficiencies above 90 % are achieved (12 V in, 3.3 V out), on this small demonstration board due to the superior level of on-resistance and thermal performance of the small SO8 footprint of Philips LFPAK devices.

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Revision history

Rev	Date	Description
01	20060302	Initial version

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1. Introduction

The LFPAK demo board demonstrates the performance of Philips LFPAK MOSFETs in an operational single-phase buck converter on a small 2.5 cm × 5.0 cm board.
The innovative SOT669 LFPAK (Loss-Free Package) has the compact footprint of the SO8 and enables a superior level of on-resistance and thermal performance by using an underside thermal pad electrically connected to the drain.

The simple, low-cost board is designed to operate from an input voltage of 12 V nominal, but is capable of operating from 5 V to 13 V. As furnished, the board output voltage, V_O, is set to 1.2 V. V_O can be adjusted from 0.8 V to 5 V by changing a resistor on the board. The LFPAK devices used on this board are the PH6325L for the control MOSFET and PH2625L for the synchronous MOSFET. The MOSFETs are rated at 25 V and have maximum R_{DSon} resistances of 6.3 mΩ and 2.6 mΩ respectively. For detailed specifications, refer to the respective MOSFET data sheets. The use of these MOSFETs allows the board to provide continuous output currents of over 25 A with adequate airflow.

Figure 1 shows the FET footprint utilized on this board. The footprint is compatible with SO8 devices allowing SO8 packages to be used on this board if desired.

The TI TPS40071 controller was selected for its feature set which includes: voltage operating range of 4.5 V to 28 V, high-side current limit, source and sink drivers, and anti-cross conduction protection. For controller technical information, see the TI data sheet for the TPS40071.

The board was designed as a simple low-cost 25 A reference design and is not intended to demonstrate the maximum performance achievable from the chosen LFPAK devices. The LFPAK devices on this board can be implemented in designs to achieve even greater output currents and efficiencies if board design and component selection (such as using a PWM controller with external high performance drivers) allow it.

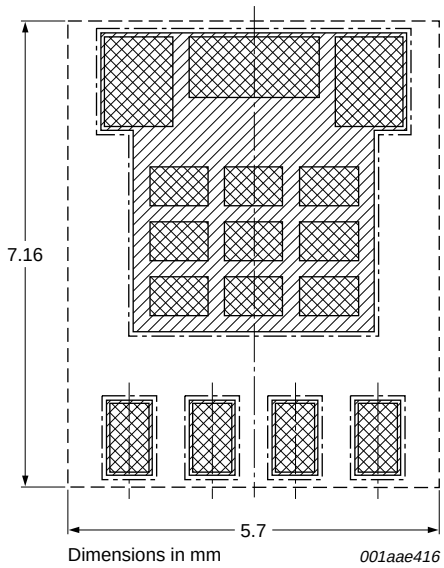

Fig 1. Simplified outline

1.1 Board top and bottom views

Figure 2 shows the top and bottom view of the board. All components are located on the topside and clearance between components is arranged so attaching meters and probes is less difficult. Power input connections, power output connections, and mounting hole pads are mirrored top and bottom.

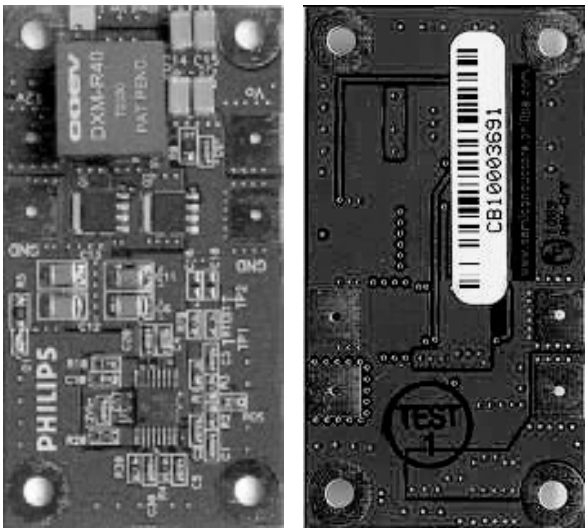

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Fig 2. Top and bottom views

1.2 Connection details

Figure 3 shows the board connections. Input power and ground connection pads are at the top of the board, and output power and ground connection pads at the bottom. The pads are large and mirrored on the board top and bottom side for current handling capability. Solder connections or alligator clips can be used to make the power attachment. Soldering to the connections pads will reduce the voltage drop of the connection. Small holes in the input and output pads are sized so that conductive posts can be inserted for oscilloscope and meter probes. Mounting-holes in the corners of the board are connected to power ground.

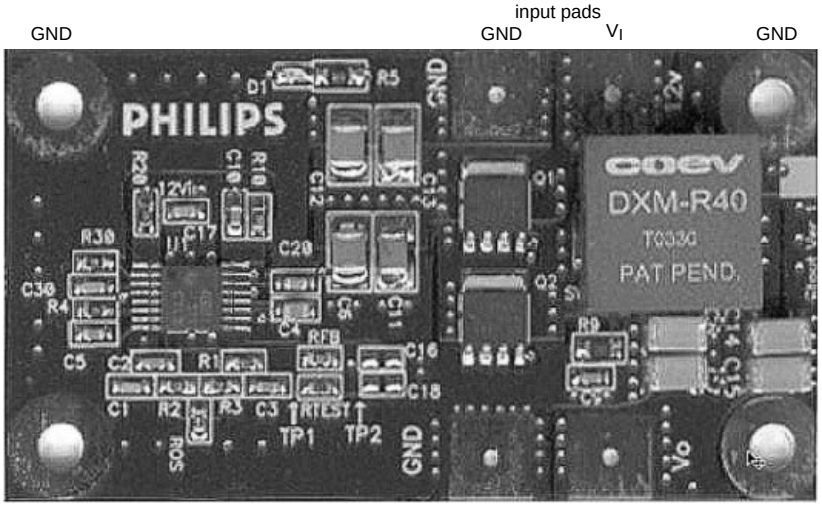


Fig 3. Input and output pads

2. Design criteria

As supplied, the board is designed to provide an output voltage of 1.2 V and 25 A. The output voltage can be changed by replacing resistor ROS. The current limits are set by R10 for operation at 1.2 V and 25 A. The operating frequency is 500 kHz. A blue status LED at the top of the board lights when the controller and board are operational. The 400 nH inductor is a 30 A device (100 °C) with a soft saturation curve, and was selected to provide good efficiency due to its low 0.9 mΩ DC resistance.

2.1 Board features

The output voltage can be easily adjusted by changing the value of a single resistor ROS. The current limit can be adjusted, as described in Section 2.1.2. Resistor R10 will need to be readjusted when changing the board V_O, if a constant current limit is to be maintained. The feedback path has been designed so that phase and gain testing can be performed by removing a single resistor. The following sections describe these features in more detail.

2.1.1 V_O selection

Replacing ROS with the values calculated in the equation below changes V_O.

$$ROS = \frac{R1 \times V_S}{V_O - V_S}$$

Where V_S is the op amp reference voltage, and is fixed at 0.7 V for the TPS40071. Resistor values for common output voltages are provided in Table 1.

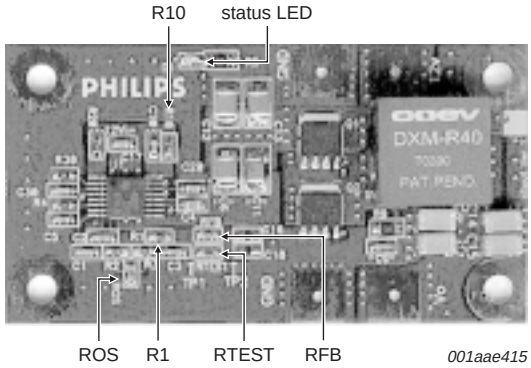


Fig 4. Location of status LED and resistors ROS, RTEST, RFB, R10 and R1

2.1.2 Control FET current limit

The TPS40071 data sheet has equations for calculating the value of R10 for a desired current limit. The TPS40071 compares voltage drop across R10 with the voltage drop across the control FET R_{DSon} at full conduction, and initiates a shutdown if the control FET exceeds the R10 voltage drop. The FET voltage drop is affected by the nominal values of V_O, V_I, temperature and output current. FET voltage drop is a direct function of R_{DSon}, and is thus temperature dependent. The blue LED will flicker during cycle-to-cycle shutdown. Please see the TPS40071 data sheet for additional information on current limit settings.

The demo board is supplied with a R10 value of 1180 Ω, typically initiating a cycle-to-cycle shutdown for currents exceeding 25 A, (case temperatures ≤ 90 °C, V_I equals 12 V). For other V_O and V_I values, the value of R10 is changed to provide this thermal protection. Table 1 should assist in the selection. Note that there is variation in shutdown current between demo boards because of variation in R_{DSon} between FETs.

Table 1. Selection of ROS and R10

V_O (V)	ROS (kΩ)	R10 (Ω)			Shutdown I_O (A)
		V_I = 12 V	V_I = 10 V	V_I = 8 V	
0.8	60.4	634	832	1180	28
1.2	12.1	1180	1540	1904	25
1.5	7.32	1400	1820	2260	22
2.5	3.32	2370	2670	2740	22
3.3	2.32	2940	3090	3090	22
5.0	1.40	2610	2610	2610	20

2.1.3 Phase and gain testing

Phase and gain testing (Bode plots) can be performed by removing the 1 Ω RFB resistor and injecting a test signal across RTEST, a 50 Ω resistor, as shown in Figure 5. By monitoring the response at TP2 to the injected signal at TP1, a phase and gain plot can be generated by varying the frequency of the test signal. The full details of this test are beyond the scope of this manual, but the measurements are easily done using a Vector Network Analyzer (VNA). Please refer to the TPS40071 data sheet for loop compensation techniques. The 1 Ω RFB resistor should remain in the circuit for normal operation.

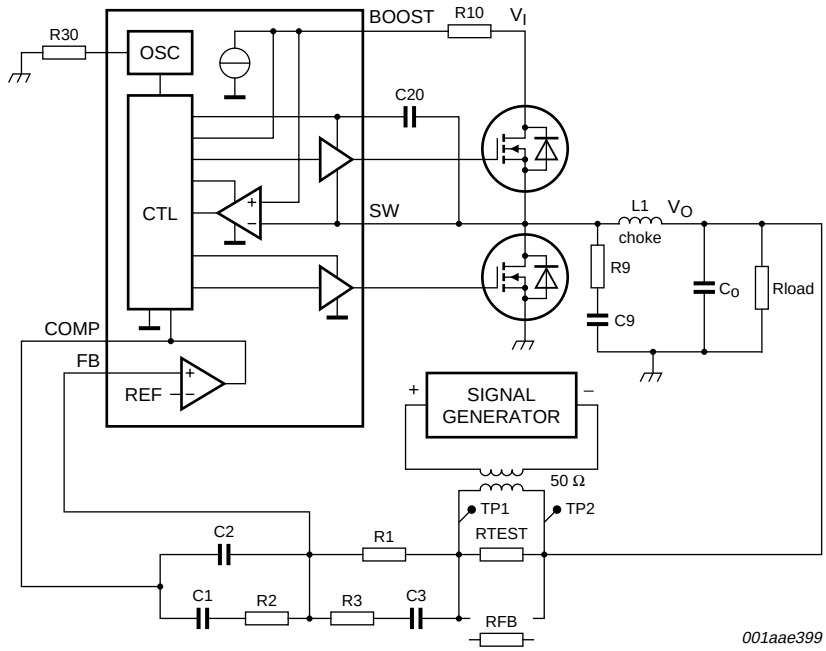
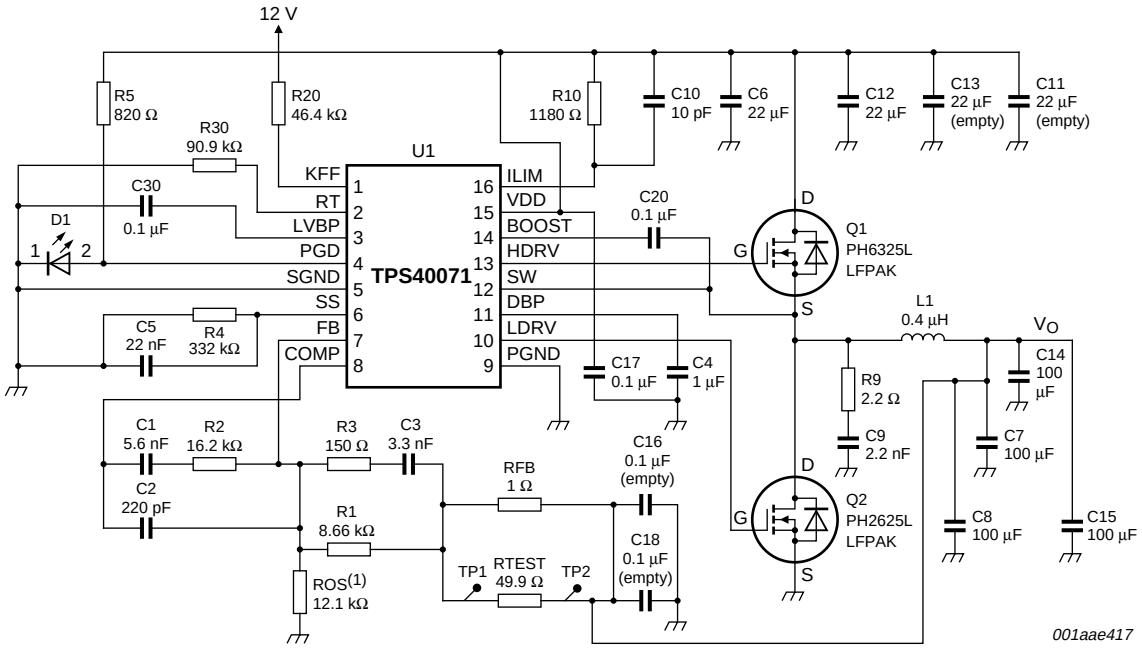


Fig 5. Phase and gain test setup

2.2 Board schematic

The board schematic is shown in Figure 6.

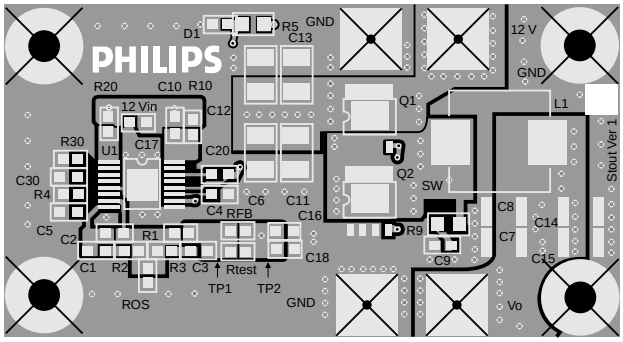


(1) ROS is set for V_O = 1.2 V; reference voltage is 0.7 V.

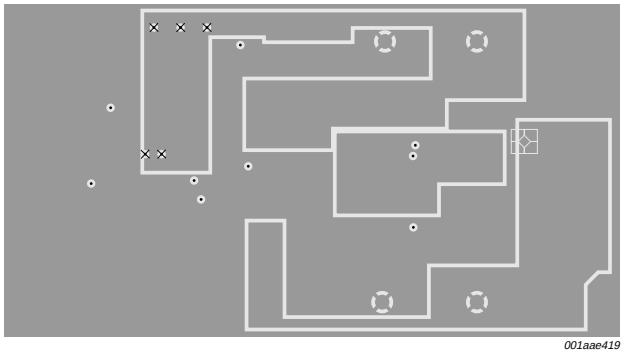
Fig 6. Schematic of the board

2.3 Layout

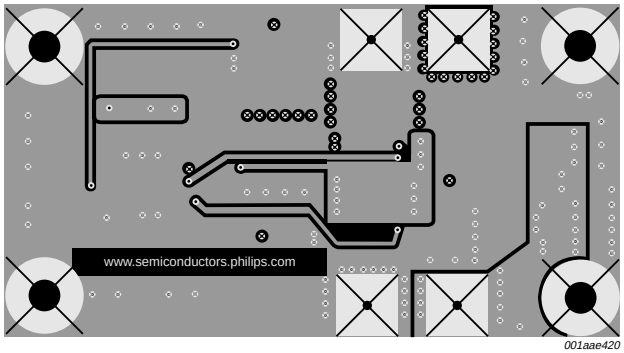
The demo board has four layers, all layers plated with 35 µm (1 oz) copper. All signals are routed top and bottom, with the inner layers servicing power and ground as shown in Figure 7. The board was designed to minimize high current induced noise in the input drive and controller circuit areas. The input current flows in a tight loop between the input pads, the input decoupling capacitors, and the MOSFETs. The output current is also confined to a separate loop. The controller is placed outside both of these high-noise power paths. The power plane splits separate high current paths from sensitive circuit areas. The ground plane is not split and uses component placement to keep noise from the switching current out of sensitive circuit areas.



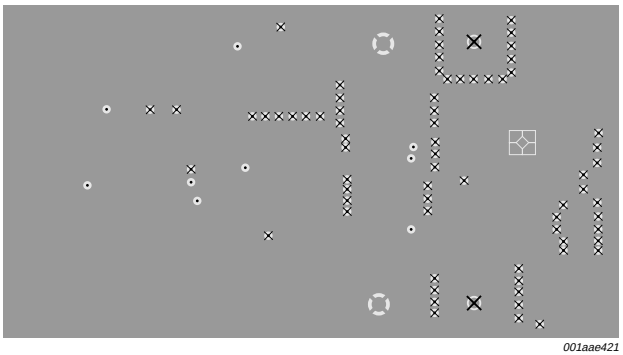
a. Top layer



b. Power layer



c. Bottom layer



d. ground layer

Fig 7. Board layouts

3. Electrical and thermal performance

The typical demo board is capable of output currents of 25 A with V_O set to 1.2 V (30 W), and 23 A with V_O set to 3.3 V (76 W). This rating is based on a 90 °C board temperature limit at 25 °C ambient and airflow of 1.0 m/s (200 LFM).

3.1 Efficiency sweeps

Efficiency is plotted in Figure 8 for V_O voltages of 1.2 V and 3.3 V. The input voltage is 12 V for both sweeps. The maximum current swept is the level that produces 90 °C FET case temperatures. Higher currents can be achieved with greater airflow. The current limit set point will need to be adjusted by changing R10 if higher currents are desired.

For a constant current output, the power output increases directly with V_O. The loss factors do not increase nearly as fast, making conversion to higher V_O values more efficient than conversion to lower V_O values.

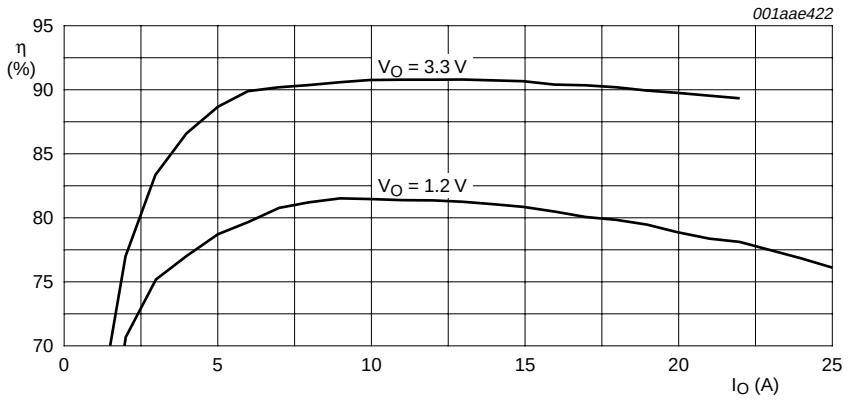
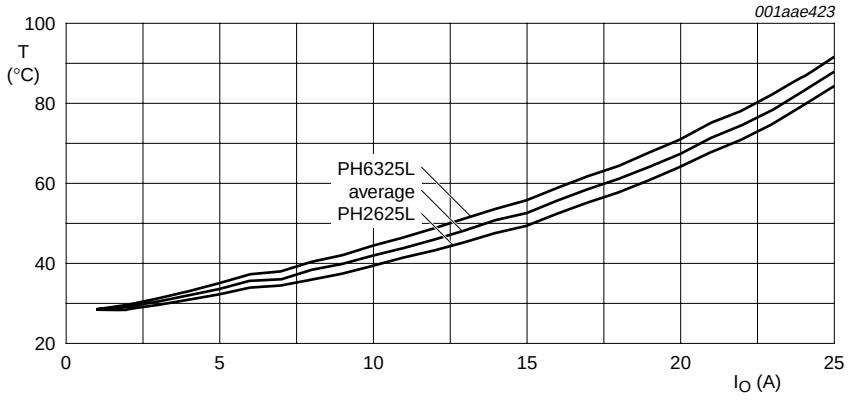


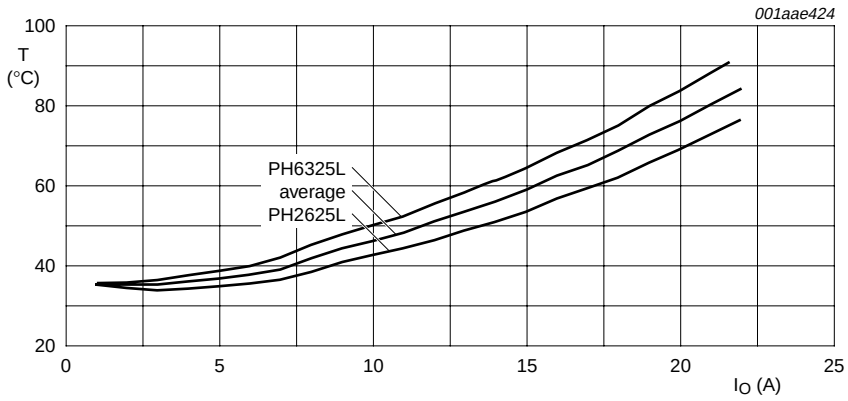
Fig 8. Efficiency sweeps for output voltages of 1.2 V and 3.3 V

3.2 Thermal sweeps

Figure 9 shows the thermal case temperature of the control and sync FETs for the efficiency sweeps in Figure 8. The load current is swept from zero to a maximum level, which is defined when the average of the two case temperatures equals 90 °C.



a. V_O = 1.2 V

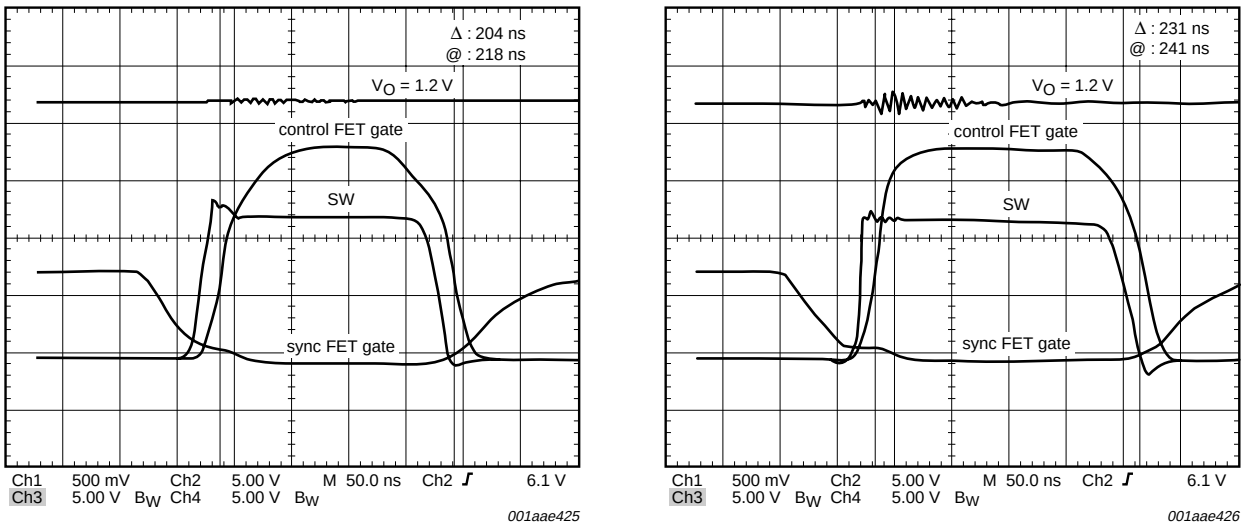


b. V_O = 3.3 V

Fig 9. Thermal measurement

3.3 Electrical waveforms

The oscilloscope plots in Figure 10 show the sync FET gate, control FET gate, and switch node for no load and 22 A load respectively.



a. no load

b. I_O = 22 A

Fig 10. Electrical waveforms

3.4 Loop gain and phase plot

Figure 11 shows the loop gain and phase as a function of frequency for V_O = 1.2 V. The compensation was very nearly the same for V_O ranges of 0.8 V to 3.3 V. The test setup is shown in Figure 5.

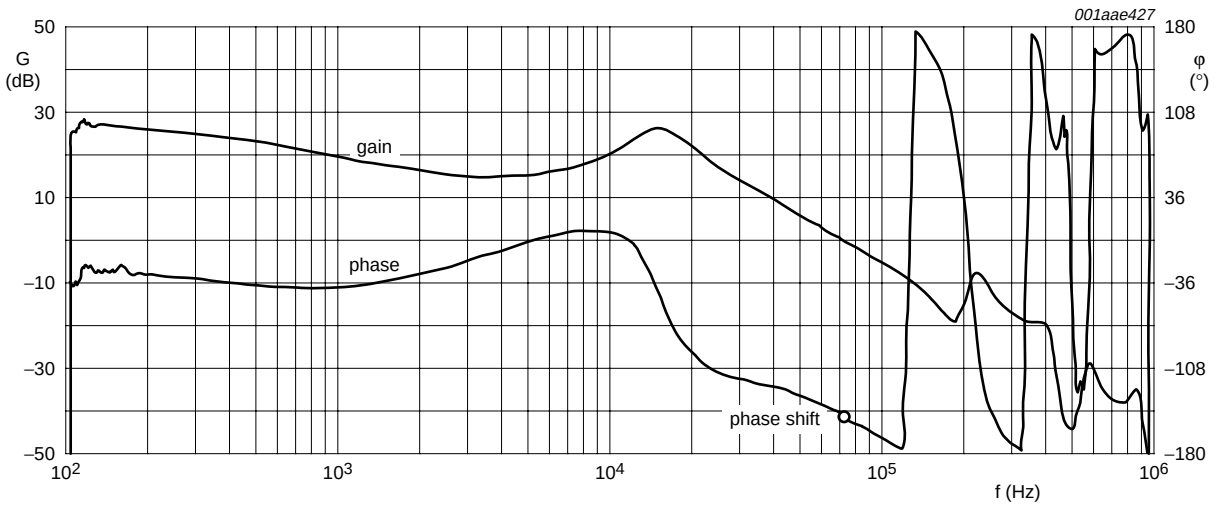


Fig 11. Phase and gain plot of demo board

4. Bill of materials

Table 2. Bill of materials

Item	Quantity	Label or value	Package	Tolerance	Rating	Manufacturer	Manufacturer PIN	Designation
1	1	3.3 nF	603	±10 %	50 V	TDK		C3
2	1	10 pF	603	±10 %	50 V	TDK		C10
3	1	220 pF	603	±10 %	50 V	TDK		C2
4	1	2.2 nF	603	±10 %	50 V	TDK		C9
5	1	22 nF	603	±10 %	50 V	TDK		C5
6	1	5.6 nF	603	±10 %	50 V	TDK		C1
7	5	0.1 µF	603	±10 %	50 V	TDK		C12, C20, C30 (C16, C18 empty)
8	1	1 µF	805	±10 %	16 V	TDK		C4
9	4	22 µF	1210	+80 % –20 %	16 V	TDK		C6, C12 (C11, C13 empty)
10	4	100 µF	1812	+80 % –20 %	6.3 V	TDK		C7, C8, C14, C15
11	1	90.9 kΩ	603	±1 %				R30
12	1	8.66 kΩ	603	±1 %				R1
13	1	332 kΩ	603	±1 %				R4
14	1	1180 Ω	603	±1 %				R10
15	1	16.2 kΩ	603	±1 %				R2
16	1	12.1 kΩ	603	±1 %				ROS
17	1	46.4 kΩ	603	±1 %				R20
18	1	150 Ω	603	±1 %				R3
19		49.9 Ω	603	±1 %				RTEST
20	1	2.2 Ω	805	±5 %				R9
21	1	820 Ω	805	±5 %				R5
22	1	1 Ω	603	±1 %				RFB
23	1	TPS40071	SOP			TI	TPS40071PWP	U1
24	1	PH6325	LFPAK		75 A	Philips	PH6325	Q1
25	1	PH2625	LFPAK		75 A	Philips	PH2625	Q2
26	1	Blue	603		3.8 V	Lite-on	LTST-C190UBKT	D1
27	1	DXM-R40	PCC MC-NX 2	±20 %	0.4 µH, 30.5 A	Coev	DXM1306-R40	L1

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Date of release: 2 March 2006

Document identifier: UM10178_1